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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/771,229	01/26/2001	Takanori Iwamatsu	FUJS 13.045A	6938
	7590 06/08/2007 CHIN ROSENMAN LLF	EXAMINER		
575 MADISON AVENUE			TSE, YOUNG TOI	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary		Application No.	Appli	Applicant(s)		
		09/771,229	IWAM	IATSU ET AL.		
		Examiner	Art Ur	nit		
		YOUNG T. TSE	2611			
7 Period for F	The MAILING DATE of this communication apple Reply	ears on the cover shee	t with the correspond	ondence address		
A SHOR WHICHI - Extensio after SIX - If NO per - Failure to Any reply	TENED STATUTORY PERIOD FOR REPLY EVER IS LONGER, FROM THE MAILING DATES of time may be available under the provisions of 37 CFR 1.136 (6) MONTHS from the mailing date of this communication. Find for reply is specified above, the maximum statutory period with the set or extended period for reply will, by statute, or received by the Office later than three months after the mailing attent term adjustment. See 37 CFR 1.704(b).	TE OF THIS COMMU6(a). In no event, however, made apply and will expire SIX (6) cause the application to become	JNICATION.  Bay a reply be timely filed  MONTHS from the mailing  The ABANDONED (35 U.S.)	ng date of this communication.		
Status		,				
1)⊠ Re	esponsive to communication(s) filed on <u>21 Ma</u>	arch 2007 and 19 July	<sup>,</sup> 2006.			
	This action is <b>FINAL</b> . 2b)⊠ This action is non-final.					
3) <u></u> Si⊢	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
clo	sed in accordance with the practice under Ex	k parte Quayle, 1935	C.D. 11, 453 O.G.	. 213.		
Disposition	of Claims	•				
4a) 5)□ Cl 6)図 Cl 7)□ Cl	aim(s) <u>1-14,47 and 48</u> is/are pending in the a Of the above claim(s) is/are withdraw aim(s) is/are allowed. aim(s) <u>1-14,47 and 48</u> is/are rejected. aim(s) is/are objected to. aim(s) are subject to restriction and/or	n from consideration.				
Application	Papers					
	e specification is objected to by the Examiner					
	e drawing(s) filed on is/are: a) acce		to by the Examin	ier.		
	plicant may not request that any objection to the d	·	•			
Re	placement drawing sheet(s) including the correction	on is required if the draw	ing(s) is objected to	o. See 37 CFR 1.121(d).		
11) Th	e oath or declaration is objected to by the Exa	aminer. Note the attac	hed Office Action	or form PTO-152.		
Priority und	ler 35 U.S.C. § 119					
a)□ . 1.[ 2.[ 3.[	Certified copies of the priority documents	have been received. have been received ity documents have been (PCT Rule 17.2(a)).	n Application No. een received in thi	**************************************		
Attachment(s)			_			
2) Notice of 3) Informati	References Cited (PTO-892) Draftsperson's Patent Drawing Review (PTO-948) on Disclosure Statement(s) (PTO/SB/08) o(s)/Mail Date	Paper 5) D Notice	ew Summary (PTO-41 No(s)/Mail Date. of Informal Patent Apple	_·		

## Reissue Applications

## Response to Arguments

1. Applicant's arguments filed on July 19, 2006 have been fully considered but they are not persuasive.

Applicants believe that remove the word "any" from the term "any one of" so that claim 47 as presented is a generic linking claim which properly links the species shown in each of figures 1-6, as recited in the original claim 1 of U. S. patent No. 5,867,542.

The examiner respectively disagrees. Although claim 47 recites the common claimed subject matter of an identifying circuit, a clock regenerating circuit, and a clock phase detecting section, as recited in the issued claims 1-14, none of the elected species of the issued claims 1-14 includes the claimed subject matter as recited in claim 47. For instance, claim 47 recites that the clock phase detecting section for detecting a phase component of signal identification clocks based on clock-phase-detecting composite input information including one of (i) a combination of a demodulated signal which is obtained by demodulating a multilevel orthogonal modulated signal and an equalized demodulated signal and (ii) a combination of clock phase difference information to be supplied to the identifying circuit and signal error differential information obtained by the identifying circuit, and then supplying the phase component to the clock regenerating circuit, and the clock phase detecting section including a difference detecting unit responsive to the receipt of the composite input information, for detecting one of (I) difference information between the demodulated signal and the

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equalized demodulated signal and (II) a combination of the clock phase difference information and the signal error differential information, and a clock phase calculating unit for calculating the phase component of said signal identification clock based on the output from the difference detecting unit. Claim 47 is generic only if claim 47 contains the conditions (i) and (I) as now recited in new claim 48, but not the conditions (ii) and (II) because the second conditions do not include at least an equalization demodulated signal, for example, generated by an equalizing circuit as required in claims 1-14 of the U. S. patent No. 5,867,542.

Therefore, none of the elected species of the issued claims 1-14 includes the claimed subject matter of an equalizing circuit, a difference detecting unit for detecting a phase component ... including the criteria of (ii) a combination of clock phase difference information to be supplied the identifying circuit and signal error difference information obtained by the identifying circuit and a difference detecting unit ... for detecting the criteria of (II) a combination of the clock phase difference information and the signal error difference information, as recited in claim 47.

2. The reissue oath/declaration filed with this application is defective because it fails to contain the statement required under 37 CFR 1.175(a)(1) as to applicant's belief that the original patent is wholly or partly inoperative or invalid. See 37 CFR 1.175(a)(1) and see MPEP § 1414.

The supplemental declaration filed on March 21, 2007 is unacceptable because the text of the supplemental declaration is illegible and unreadable.

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Applicants belief that an error has been made by reason of the patentees claiming less than they had the right to claim in the patent. In particular, the patentees concluded that a generic claim could have been included among the claims during prosecution of the elected species.

Had a generic claim been entered and allowed in the parent case, then following allowance of the elected claims, the examiner would have examined a reasonable number of additional species. Failure to have additional species examined in the parent case was the penalty paid for the error of omitting a generic claim. The reissue application has the objective of rectifying that error and defining a generic claim and thereby also cover hopefully all species that were originally claimed in the parent application.

The amended claim 47 recites the common claimed subject matter of an identifying circuit, a clock regenerating circuit, and a clock phase detecting section, as recited in the issued claims 1-14, none of the elected species of the issued claims 1-14 includes the claimed subject matter as recited in the amended claim 47. For instance, claim 47 recites that the clock phase detecting section for detecting a phase component of signal identification clocks based on clock-phase-detecting composite input information including one of (i) a combination of a demodulated signal which is obtained by demodulating a multilevel orthogonal modulated signal and an equalized demodulated signal and (ii) a combination of clock phase difference information to be supplied to the identifying circuit and signal error differential information obtained by the identifying circuit, and then supplying the phase component to the clock regenerating

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circuit, and the clock phase detecting section including a difference detecting unit responsive to the receipt of the composite input information, for detecting one of (I) difference information between the demodulated signal and the equalized demodulated signal and (II) a combination of the clock phase difference information and the signal error differential information, and a clock phase calculating unit for calculating the phase component of said signal identification clock based on the output from the difference detecting unit.

Claim 47 is generic only if claim 47 contains the conditions (i) and (I) as now recited in new claim 48, but not the conditions (ii) and (II) because the second conditions do not include at least an equalization demodulated signal, for example, generated by an equalizing circuit as required in claims 1-14 of the U. S. patent No. 5,867,542.

Therefore, none of the elected species of the issued claims 1-14 includes the claimed subject matter of an equalizing circuit, a difference detecting unit for detecting a phase component ... including the criteria of (ii) a combination of clock phase difference information to be supplied the identifying circuit and signal error difference information obtained by the identifying circuit and a difference detecting unit ... for detecting the criteria of (II) a combination of the clock phase difference information and the signal error difference information, as recited in claim 47.

However, according to MPEP 1450 Restriction and Election of Species. A reissue applicant's failure to timely file a divisional application is not considered to be the error causing a patent granted on elected claims to be partially inoperative by

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reason of claiming less than the applicant had a right to claim. Thus, such error is not correctable by reissue of the original patent under 35 U.S.C. 251. In re Watkinson, 900 F.2d 230, 14 USPQ2d 1407 (Fed. Cir. 1990); In re Orita, 550 F.2d 1277, 1280, 193 USPQ 145, 148 (CCPA 1997). See also In re Mead, 581 F. 2d 251, 198 USPQ 412 (CCPA 1978). Likewise, if the original patent specification or the prosecution history of the original patent shows an intent <u>not to claim</u> the newly presented invention, that invention cannot be added by reissue.

3. Claims 1-14 and 47 are rejected as being based upon a defective reissue declaration under 35 U.S.C. 251 as set forth above. See 37 CFR 1.175.

The nature of the defect(s) in the declaration is set forth in the discussion above in this Office action.

#### Claim Objections

4. Claims 8-14 are objected to because of the following informalities:

In claim 8, line 14, the term "an input signal to output signal error" should be "the input and output signals".

In claim 11, line 8, "identifying circuits" should be "plural identifying circuits".

The dependent claims 9-10 and 12-14 depend upon the independent claim 8.

Appropriate correction is required.

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#### Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
- 7. Claims 1 and 47-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lim (U. S. Patent No. 5,423,085) in view of Kobayashi (U. S. Patent No. 5,535, 252).

Lim discloses an automatic frequency control method in Fig. 2 and an apparatus in Fig. 3 for performing the method includes an equalizer (301), a channel characteristic estimator (302), a re-modulator (303), a phase comparator (304), a frequency error estimator (305) and a digital-to-analog converter (306) for converting digital signal into analog signal to a LPF and a VCO, thus improve the receiving performance of a receiver by digital implementation.

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Regarding claims 1 and 47-48, the receiver comprises the automatic frequency control circuit of Fig. 3 comprising an identifying circuit (A/D converter 202) for identifying a demodulated signal at a predetermined identification level, the demodulated signal being obtained by demodulating a multilevel orthogonal modulated signal; a clock regenerating circuit (VCO) for regenerating a signal identification clock; an equalizing circuit (301) for subjecting the demodulated signal obtained by demodulating the multilevel orthogonal modulated signal to an equalizing process; and a clock phase detecting unit (303, 304, 305) for detecting a phase component of the signal identification clock based on errors between input and output signals of the equalizing circuit and then for supplying the phase component to the VCO through the DAC (306) and the LPF; wherein said clock phase detecting unit includes: an error detecting unit (304) for detecting a signal error between the input and output signals of said equalizing circuit; and a clock phase calculating unit (305) for detecting the phase component of the signal identification clock by calculating the detection outputs from the error detecting unit.

Although Lim does not explicitly show or suggest that the signal identifying clock generated by the VCO is used to control the A/D converter, it is well to a person skill in the art that an automatic frequency control circuit in general is used to control the frequency or clock signal of an analog-to-digital converter. For example, Kobayashi discloses a receiver circuit in Fig. 2 comprising a frequency control circuit including a clock reproducing circuit (48) for generating a signal identifying clock to the A/D converter (41 and 42) or identifying circuit.

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Therefore, it would have been obvious to one of ordinary skill in the art that the signal identifying clock generated by the VCO of Lim's automatic control circuit is capable of controlling the A/D converter in order to identify the clock/frequency of a converter circuit, for example, also taught by Kobayashi.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-30513051. The examiner can normally be reached on Monday-Thursday and alternative Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The Central FAX Number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YOUNG T. TSE Primary Examiner Art Unit 2611